DPU – Data Processing Unit

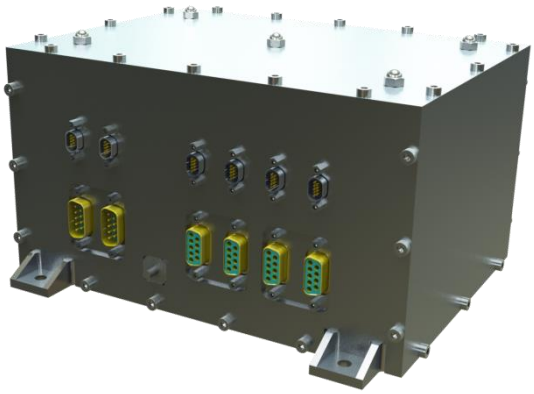
AMDL S.r.l. – www.amdl.biz

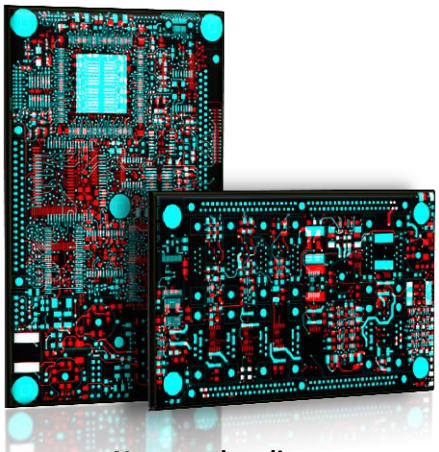
Our own DPU introduces, for the first time in a flight ECSS design, the outstanding Aeroflex dual Leon 3FT core GR712RC part (ITAR FREE*), just made available and qualified for the space market

The processor natively provides up to 6 complete Spacewire cores each plus a large number of standard I/F protocols.

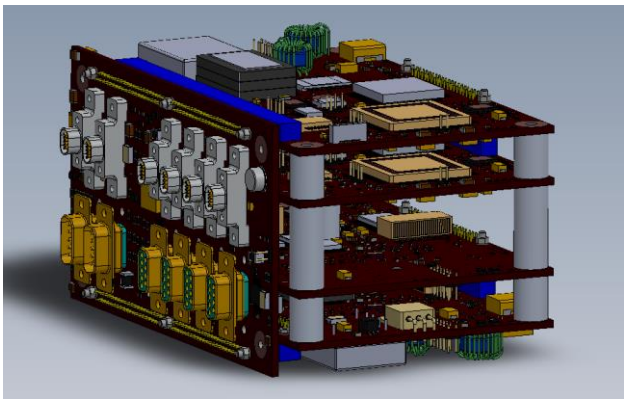
Dual-Core LEON 3FT SPARK V8 32-bit

In our configuration a stack of dual processors boards present in each active set of DPU (Main or Redundant) allow to extend up to 12 SpaceWire interfaces and to gain a double computational capability. The configuration foresees as well the full doubling of the stack to guarantee a complete cold redundancy of the unit.





New product line
Main / Ancillary by configuration switch and the master I/F board (on the right)



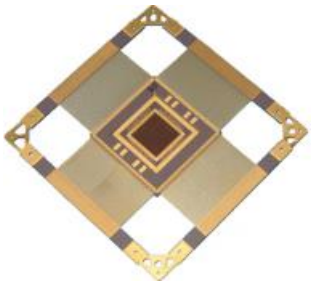
The complete board stack.
This model optimizes thermal balancing and structural and eliminate completely the need of any internal harness

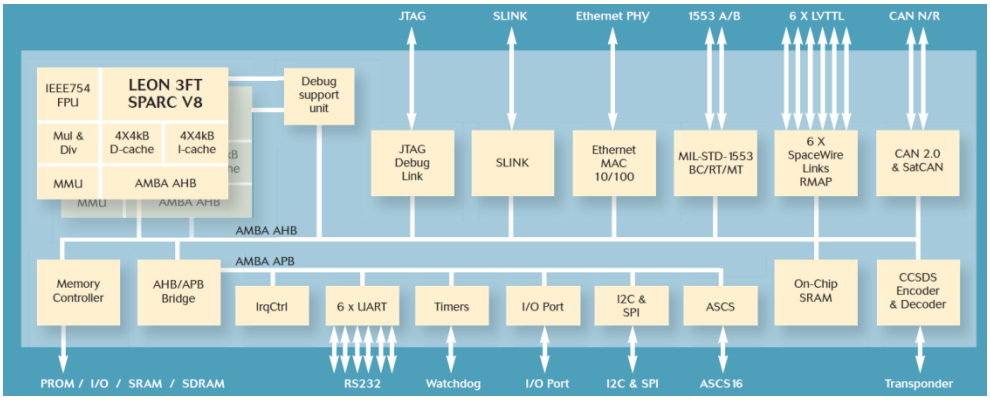
***ITAR**: International Traffic in Arms Regulations is a set of United States government regulations that control the export and import of defense-related articles and services on the United States Munitions List (USML)

See more at http://pmddtc.state.gov/regulations_laws/itar_official.html

The CPU core

Core LEON 3FT SPARC™ V8 32-Bit Microprocessor
GR712RC Dual-Core LEON 3FT Microprocessor
Designed for operation in harsh environments
Fault Tolerant architecture
Guaranteed radiation performance
Real-time multiprocessing support





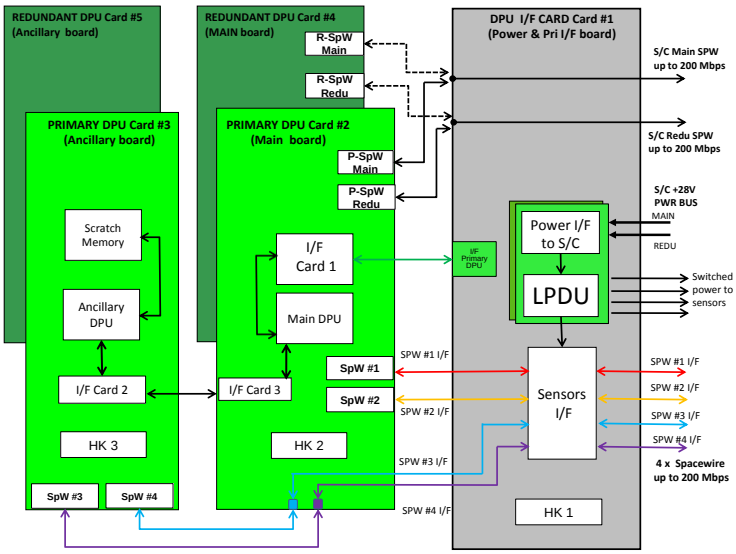
	SDRAM (with RS)	UART 0	UART 1	UART 2	UART 3	UART 4	UART 5	SpaceWire 0	SpaceWire 1	SpaceWire 2	SpaceWire 3	SpaceWire 4	SpaceWire 5	Ethernet	CAN	SATCAN	MIL-STD-1553B	I2C	SPI	SLINK	ASCS	CCSDS TC 0	CCSDS TC 1	CCSDS TC 2	CCSDS TC 3	CCSDS TC 4	CCSDS TM
SDRAM (with RS)	-										X	X															
UART 0		-																									
UART 1			-																								
UART 2				-																							
UART 3					-																						
UART 4						-																					X
UART 5							-															X					X
SpaceWire 0								-																			
SpaceWire 1									-																		
SpaceWire 2										-					X	X					X						
SpaceWire 3											-								X								
SpaceWire 4	X											-									X	X					
SpaceWire 5	X												-			X						X	X				
Ethernet														-	X	X	X						X	X			
CAN										X				X	-												
SATCAN										X			X	X		-	X					X	X	X			
MIL-STD-1553B													X		X	-					X		X	X			
I2C																		-								X	
SPI																			-	X					X		
SLINK											X								X	-					X		
ASCS										X		X					X				-	X					
CCSDS TC 0							X					X	X		X						X	-					
CCSDS TC 1													X	X		X	X						-				
CCSDS TC 2														X		X	X							-			
CCSDS TC 3																			X	X					-		
CCSDS TC 4																		X								-	
CCSDS TM						X	X																				-

High computational capability solution

In order to have a more flexible product CPU clock can be scaled up to 100MHz frequency or 200MIPS peak.
Moreover a switches array allows to selected different standard of I/Fs to connect the system to other systems such us LAN, 1553 etc.

Images are courtesy of *Aeroflex* GR712RC Brochure

The DPU design supports a cold redundancy DPU design and has been developed on four standard 100x160mm^2 euro cards and a 90x160 mm^2 motherboard card



- I/F common motherboard card
- Primary Main DPU card
- Primary Ancillary DPU card
- Redundant Main DPU card
- Redundant Ancillary DPU card

This device is an implementation of the dual-core LEON3FT SPARC V8 processor using RadSafeTM technology. Each processor core includes a SPARC Reference Memory Management Unit (SRMMU) and an IEEE-754 compliant double-precision FPU for floating-point operations. It can be utilized in symmetric or asymmetric multiprocessing mode. The GR712RC architecture is centred around the AMBA Advanced High-speed Bus (AHB), to which the two LEON3-FT processors and other high-bandwidth units are connected. Low-bandwidth units are connected to the AMBA Advanced Peripheral Bus (APB) which is accessed through an AHB to APB bridge. The part is provided in a 240-pin, 0.5 mm pitch high-reliability ceramic quad flat package (CQFP). Further important resources have been housed on the board apart the 28V DC-DC converter :

- 20 Megabit (512K x 40-Bit) EEPROM, available both on Main and Ancillary cards.
- 512k x 40, Rad Hard Low Power CMOS SRAM 15 ns/3.3V available both on Main and Ancillary cards.
- 3 Gb 128Mx24SDRAM based scratch memory +2 Gb 128Mx16 SDRAM based scratch memory , available on Ancillary cards.

The DPU components part list is ESA/SCC qualified

PART TYPE	QUALITY SCREENING LEVEL
Microcircuits	ESA/SCC Class B MIL-PRF-38535 Class V
Hybrids	ESA-PSS-608 Class B: MIL-PRF Class K (US manufacturers only)
Transistors / Diodes / Optos	ESA / SCC Class B MIL-PRF-19500 Class S
Critical Passive Components (Crystals, relays, filters, CCD, Connector, Cable)	ESA / SSC Class B
Passive Components	ESA / SSC Class C MIL failure rate R or B

100 Krad radiation tolerant

DPU mass budget

DPU Electronics Box			
ITEM	MASS [g]	Contingency 20% [g]	Mass incl. Cont. [g]
	524,39	104,88	629,27
DPU Electronics Cards + locking screws + bearings			
	1202,34	240,47	1442,81
TOT DPU without cont. [g]			1726,73
Cont 20% [g]			345,35
TOT DPU incl. Cont. [g]			2072

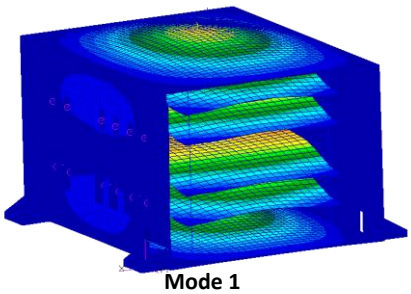
DPU power budget

ITEM	CBE POWER
Total DPU Boards (Main + Redu + I/F)	4382 mW
DC-DC (73% eff) heat	1621 mW
Total DPU	6003 mW

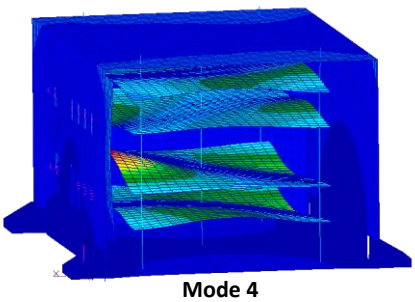
DPU mechanical and thermal analysis

Mode	Freq (Hz)	Mx (%)	My (%)	Mz (%)	Ixx (%)	Iyy (%)	Izz (%)
1	184,03	-	52,5%	-	27,3%	-	27,5%
2	259,94	-	-	37,2%	19,3%	14,8%	-
4	287,33	43,8%	-	-	-	11,4%	23,5%
5	287,79	8,1%	-	-	-	2,1%	4,2%
7	315,73	17,8%	-	-	-	2,5%	-
10	342,15	-	5,0%	2,0%	-	-	2,7%
16	373,94	-	-	5,0%	3,7%	2,5%	-
18	380,31	-	-	4,3%	3,2%	1,2%	-
19	388,04	-	-	8,9%	6,2%	3,2%	-
20	395,28	-	-	3,3%	2,6%	1,9%	-
21	430,71	-	4,8%	5,1%	2,7%	1,9%	3,0%
36	567,90	-	4,4%	1,5%	1,5%	1,8%	-
Total at 2000 Hz		85,1%	98,1%	84,3%	97,7%	75,5%	98,2%

Modal analysis



Mode 1



Mode 4

Sine analysis

X

Id.	Material	s_{MAX} (MPa)	$MOS_{Ultimate}$	MOS_{Yield}
DPU Box	Al 6082-T681	24.80	4.95	6.74
PCBs	Polyimide	3.41	35.66	-
Bars	AISI 316	73.50	2.74	1.61

Y

Id.	Material	s_{MAX} (MPa)	$MOS_{Ultimate}$	MOS_{Yield}
DPU Box	Al 6082-T681	19.60	6.53	8.80
PCBs	Polyimide	6.78	17.44	-
Bars	AISI 316	48.20	4.71	2.98

Z

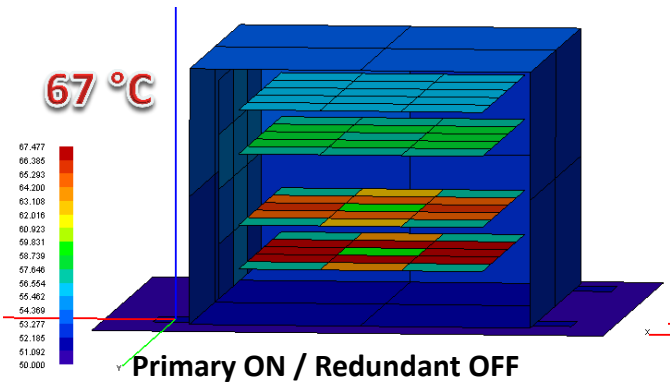
Id.	Material	s_{MAX} (MPa)	$MOS_{Ultimate}$	MOS_{Yield}
DPU Box	Al 6082-T681	64.10	1.30	2.00
PCBs	Polyimide	20.50	5.10	-
Bars	AISI 316	22.00	11.50	7.73

Random analysis

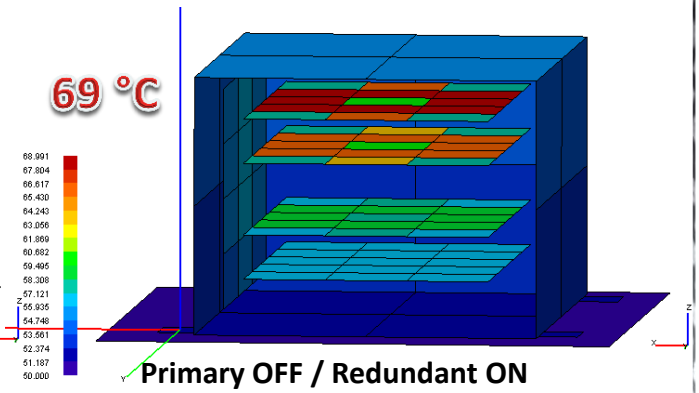
Id.	Material	s_{MAX} (MPa)	$MOS_{Ultimate}$	MOS_{Yield}
DPU Box	Al 6082-T681	7.94	17.58	23.18
PCBs	Polyimide	4.72	25.48	-
Bars	AISI 316	20.70	12.29	8.28

Id.	Material	s_{MAX} (MPa)	$MOS_{Ultimate}$	MOS_{Yield}
DPU Box	Al 6082-T681	8.82	15.72	20.77
PCBs	Polyimide	5.58	21.40	-
Bars	AISI 316	21.80	11.61	7.81

Id.	Material	s_{MAX} (MPa)	$MOS_{Ultimate}$	MOS_{Yield}
DPU Box	Al 6082-T681	20.60	6.16	8.32
PCBs	Polyimide	6.51	18.20	-
Bars	AISI 316	5.50	49.00	33.91

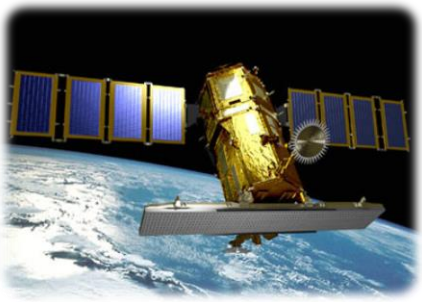


Primary ON / Redundant OFF

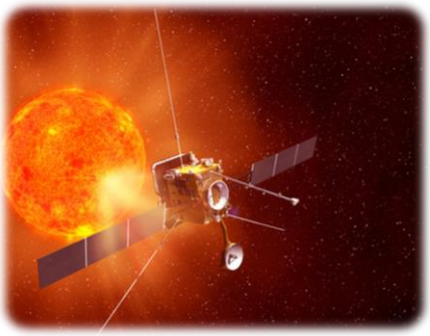


Primary OFF / Redundant ON

Application fields

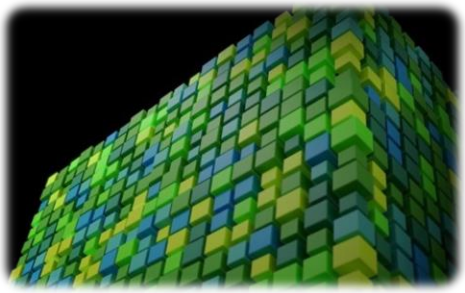


Data compression for imaging sensors



Hardware/software high reliability and high performance calculations for scientific satellites

High precision calculations: IEEE-754 compliant double-precision FPU for floating-point operations.



High volume data management

Multi sensors support: 6 or more SpaceWire links

DPU software customizations

The DPU can offer customized real-time operative system and on board massive data compression such:

- SemiLog compression
- Hartmann Quad Tree
- Rice
- JPEG and JPEG-2000
- ESA CCSDS 122.0-B-1 compression codes

The Consultative Committee for Space Data Systems

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